Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for erasing non-volatile memory cells in an integrated non-volatile memory device that comprises a memory cell array organized in a row-and-column layout, and divided in array sectors, the method comprising:

forcing an incompletely erased sector into a read condition;

scanning rows of said sector to check for possible presence of a spurious current indicating a fail state;

identifying and selectively electrically isolating a failed row associated with the fail state, the electrical isolating including placing the failed row in a floating state by decoupling the failed row from first and second power supplies of different polarity;

re-addressing from said failed row to a redundant row within a threshold distance of the failed row; and

re-starting an erase algorithm.

2. (Previously Presented) A method according to claim 1 wherein said read condition is forced whenever a result of the erase algorithm is incomplete or negative.

3. (Previously Presented) A method according to claim 1 wherein rows of a given sector are scanned, also checking for possible presence of said spurious discharge current in a conduction path leading to a positive power.

4. (Previously Presented) A method according to claim 1 wherein at least one switch is provided between each decode block and respective positive and negative power

supplies, respectively comprising the first and second power supplies, in order to isolate the failed row.

5. (Previously Presented) A method according to claim 1 wherein said re-addressing is effected using a redundancy decode block incorporated inside row decode circuitry.

6. (Previously Presented) A method according to claim 4 wherein said switches are driven by a logic operatively interlinked to contents of redundancy registers.

7. (Previously Presented) A method according to claim 3 wherein said spurious current is detected by comparison of a row node with a redundancy node.

8. (Previously Presented) A method according to claim 7 wherein said comparison is effected by a compare block, to which is input a reference signal produced from a redundant row and a row signal taken at a beginning of a row being scanned.

9. (Previously Presented) The method according to claim 1 wherein the redundant row is adjacent to a sector containing the failed row.

10. (Previously Presented) The method according to claim 1 wherein the redundant row is in a same sector as a sector containing the failed row.

11. (Currently Amended) An integrated non-volatile memory device of the programmable and electrically erasable type, comprising a memory cell array organized in a row-and-column layout, and divided in array sectors, each including at least one row decode circuit portion being supplied positive and negative voltages, the device comprising:

a redundant row block inside each sector;

a plurality of row decode blocks and at least one redundancy decode block within the decode circuitry; and

at least one switch between each one of the decode blocks and the respective positive and negative voltages in order to selectively isolate a failed row during read, program or erase operations, including capability of the switches to place the failed row in a floating state by respectively decoupling the failed row from the positive and negative voltages.

12. (Previously Presented) A device according to claim 11 wherein said switches are MOS transistors.

13. (Previously Presented) A device according to claim 11, further comprising control logic for controlling said switches.

14. (Previously Presented) A device according to claim 13 wherein operation of said logic is interlinked with contents of redundancy registers.

15. (Previously Presented) A device according to claim 11, further including a comparing block, the comparing block receiving an input reference signal produced by a redundant row and a row signal taken at a start of a row being scanned.

16. (Previously Presented) A method for erasing non-volatile memory cells, the method comprising:

dividing a non-volatile memory device in array sectors;

forcing an incompletely erased sector into a read condition;

scanning rows of said sector;

comparing a row node with a redundancy node to check for possible presence of a spurious current indicating a fail state;

identifying and electrically isolating a failed row associated with the fail state;

re-addressing from said failed row to a redundant row, the redundant row being within a threshold distance of the failed row; and

re-starting an erase algorithm.

17. (Previously Presented) A method according to claim 16 wherein said comparison is effected by a compare block that receives a reference signal produced from a redundant row and a row signal taken at a beginning of a row being scanned.

18. (Previously Presented) An integrated non-volatile memory device of the programmable and electrically erasable type, the memory device comprising:

a memory cell array organized in a row-and-column layout and divided in array sectors, each of the memory cell arrays having at least one row decode circuit portion coupled to first and second potentials;

a redundant row block inside each sector;

a plurality of row decode blocks and at least one redundancy decode block within the decode circuitry;

a comparing block, the comparing block receiving a reference signal produced by the redundant row and a row signal taken at a start of a row being scanned; and

at least one switch between each one of the decode blocks and the respective first and second potentials in order to isolate a failed row during read, program and erase operations.

19. (Previously Presented) The device of claim 11 wherein other rows in a same sector as the failed row continue to be supplied with the positive and negative voltages, while the failed row is in the floating state.

20. (Previously Presented) The memory device of claim 18 wherein other rows in a same sector as the failed row continue to be supplied with the first and second potentials, while the failed row is in the isolated and floating state.

21. (Previously Presented) The memory device of claim 18 wherein the first and second potentials respectively comprise positive and negative potentials.

22. (New) The method of claim 1 wherein selectively electrically isolating the failed row includes selectively electrically isolating the failed row while other rows in said sector continue to be powered by said first and second power supplies.